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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/505,949	CHOW ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been considered. Claims 1-10, 18, and 19 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 13 April 2007.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-4, 8-10, 15, and 17-19 are rejected under 35 U.S.C. 102(e) as being taught by Guenthner, U.S. Patent Number 6,448,676 (herein referred to as Guenthner).

5. Referring to claim 1, Guenthner has taught a multi-mode processor comprising:

   a. A first instruction set engine to process instructions from a first instruction set architecture (ISA), the first ISA designed for a first processor having a first word size that defines the maximum number of bits that the first processor can handle as a single unit (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six

(36) bit system. Another proprietary thirty-six (36) bit system…A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "…This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot…"; column 8, lines 22-48 "…processors **50'**, **50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions…"; Figure 5; and Figure 6);

b. A second instruction set engine to process instructions from a second ISA, the second ISA designed for a second processor having a second word size that defines the maximum number of bits that the second processor can handle as a single unit, the second word size being different than the first word size (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions…"; column 1, lines 16-20 "…computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "…proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system…A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "…This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot…"; column 8, lines 22-48 "…processors **50'**, **50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions…"; Figure 5; and Figure 6);

c. A mode identifier (Guenthner column 5, lines 46-55 "…efficiently distinguish the two (or more) types of instructions that can execute…" – In regards to Guenthner,

a mode identifier is whatever the decoder uses to identify which instruction set the current instruction is from.);

d. A plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5 – In regards to Guenthner, both the 36 bit and 64 bit floating-point units in Figure 5 make-up the floating-point unit for the entire system, i.e. both of the individually shown units are necessary to execute floating-point instructions in the entire system.); and

e. A floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5).

6. Referring to claim 3, Guenthner has taught the multi-mode processor of Claim 1 wherein the floating-point unit comprises:

a. Pre-processing hardware to detect if a token exists in the input (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.);

b. An arithmetic unit responsive to the input and the mode identifier (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5 – In regards to Guenthner, the floating-point unit of the entire system processes instructions sent to it by the decoder after determining which type of floating-point instruction and from which instruction set.); and

c. Post-processing hardware to perform a token specific operation if a token exists in the input (Guenthner column 4, line 40 to column 5, line 22; Figure 3; and Figure 4 – In regards to Guenthner, the translation that must be done to convert from narrow to wide is true not only for instruction but also for data, such as Narrow data, e.g. 36 bit instruction data results, being written to Wide data memory, e.g. 64 bit registers.).

7. Referring to claim 4, Guenthner has taught the multi-mode processor of Claim 1 wherein the input includes data stored in at least one of the floating-point registers (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5).

8. Referring to claim 8, Guenthner has taught the multi-mode processor of Claim 1 wherein the mode identifier indicates whether the processor is in a first mode or a second mode (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of

instructions that can execute..." – In regards to Guenthner, a mode identifier is whatever the decoder uses to identify which instruction set the current instruction is from.).

9. Referring to claim 9, Guenthner has taught the multi-mode processor of Claim 1 wherein the mode identifier indicates whether the processor is in a 32 bit word ISA mode or a 64 bit word ISA mode (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot..."; column 8, lines 22-48 "...processors **50'**, **50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions..."; Figure 5; and Figure 6 – In regards to Guenthner, while the specification uses 36 bit instruction set as the main example throughout the exemplary embodiment, however, column 4, lines 25-31 states "It should be noted that this invention covers other combinations of 'NARROW' and "WIDE' architectures. For example, most micro-processors presently utilize thirty-two (32) bit architectures..." showing that the 36 bit size is just an example and 32 bits can be used as well.).

10. Referring to claim 10, Guenthner has taught a method in a multi-mode processor comprising:

a. Fetching an input from at least one of a plurality of floating-point registers (Guenthner column 6, lines 24-36 "...floating-point registers **96** are

bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5);

b. Detecting whether the input contains a token (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.);

c. If the token is detected in the input, checking what mode the processor is in (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.);

d. When the mode the processor is in is a first word size instruction set architecture (ISA) mode, processing the input to render an arithmetic result, the first ISA designed for a first processor having the first word size that defines the maximum number of bits that the first processor can handle as a single unit (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot..."; column 8,

lines 22-48 "...processors **50'**, **50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions..."; Figure 5; and Figure 6);

e. When the mode the processor is in is a second word size ISA mode, performing a token specific operation, the second word size ISA designed for a second processor having the second word size that defines the maximum number of bits that the second processor can handle as a single unit, the second word size being different than the first word size (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot..."; column 8, lines 22-48 "...processors **50'**, **50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions..."; Figure 5; and Figure 6 – In regards to Guenthner, when in Narrow mode, the system must perform specific operations to fit the wide system requirements.); and

f. Producing an output based upon the mode the processor is in (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and

utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5).

11. Referring to claim 12, Guenthner has taught the method of Claim 10 wherein processing comprises executing at least one operation on the at least one operand according to the at least one operator to achieve a result (Guenthner column 3, lines 22-63 "The instruction cache **56** is coupled to and provides instructions to an instruction execution unit **52**..."; column 5, line 56 to column 6, line 36 "...The execution unit **82** provides control signals..."; and Figure 5 – In regards to Guenthner, instructions inherently have at least one operand and at least one operator. Please see the accompanying information about instructions.).

12. Referring to claim 15, Guenthner has taught the method of Claim 10 wherein checking comprises checking a mode identifier (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, a mode identifier is whatever the decoder uses to identify which instruction set the current instruction is from.).

13. Referring to claim 17, Guenthner has taught the method of Claim 11 wherein the first mode is a 32 bit word ISA mode and the second mode is a 64 bit word ISA mode (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot..."; column 8, lines

22-48 "...processors **50', 50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions..."; Figure 5; and Figure 6 – In regards to Guenthner, while the specification uses 36 bit instruction set as the main example throughout the exemplary embodiment, however, column 4, lines 25-31 states "It should be noted that this invention covers other combinations of 'NARROW' and "WIDE' architectures. For example, most micro-processors presently utilize thirty-two (32) bit architectures..." showing that the 36 bit size is just an example and 32 bits can be used as well.).

14. Referring to claim 18, Guenthner has taught a multi-mode processor comprising:

a. A plurality of instruction set engines to process instructions from a plurality of instruction set architectures, the plurality of instruction set architecture each designed for a respective processor having a different word size that defines the maximum number of bits that the respective processor can handle as a single unit (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot..."; column 8, lines 22-48 "...processors **50', 50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions..."; Figure 5; and Figure 6);

b. A mode identifier (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, a mode identifier is whatever the decoder uses to identify which instruction set the current instruction is from.);

c. A plurality of floating-point registers shared by the instruction set engines (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5 – In regards to Guenthner, both the 36 bit and 64 bit floating-point units in Figure 5 make-up the floating-point unit for the entire system, i.e. both of the individually shown units are necessary to execute floating-point instructions in the entire system.); and

d. A plurality of floating-point units coupled to the floating-point registers, the floating-point units processing an input responsive to the mode identifier (Guenthner column 6, lines 24-36 "...floating-point registers **96** are bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5).

15. Referring to claim 19, Guenthner has taught a method in a multi-mode processor comprising:

a. Fetching an input from at least one of a plurality of floating-point registers (Guenthner column 6, lines 24-36 "...floating-point registers **96** are

bidirectionally coupled to and utilized by the thirty-six (36) bit floating-point unit **68** and the sixty-four (64) bit floating-point unit **98**..." and Figure 5);

b. Detecting whether the input contains at least one token of a plurality of tokens (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.);

c. If at least one token is detected in the input, checking what mode the processor is in (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.);

d. Processing the input to render an arithmetic result when the processor is in at least a first word size instruction set architecture (ISA) mode of a plurality of word size ISA modes, a first ISA designed for a first processor having a first word size that defines the maximum number of bits that the first processor can handle as a single unit (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions..."; column 1, lines 16-20 "...computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "...proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system...A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "...This thirty-

six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot…"; column 8, lines 22-48 "…processors **50', 50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions…"; Figure 5; and Figure 6); and

e. Performing a token specific operation when the processor is in at least a second word size ISA mode of the plurality of word size ISA modes, the second ISA designed for a second processor having a second word size that defines the maximum number of bits that the second processor can handle as a single unit, the second word size being different than the first word size (Guenthner Abstract "A data processing system contains a processor supporting both Narrow and Wide instructions…"; column 1, lines 16-20 "…computer processor capable of supporting 32, 36, or 48 bit industry standard busses and peripherals."; column 1, lines 24-30 "…proprietary thirty-six (36) bit system. Another proprietary thirty-six (36) bit system…A number of companies sell proprietary thirty-two (32) bit systems."; column 4, lines 5-32 "…This thirty-six (36 bit processor can plug into an industry standard sixty-four (64) bit processor slot…"; column 8, lines 22-48 "…processors **50', 50"** capable of executing both thirty-six (36) bit "NARROW" and sixty-four (64) bit "WIDE" instructions…"; Figure 5; and Figure 6 – In regards to Guenthner, when in Narrow mode, the system must perform specific operations to fit the wide system requirements.).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2, 5, 7, 11, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guenthner, U.S. Patent Number 6,448,676 (herein referred to as Guenthner), as applied to claims 1 and 10 above, and further in view of Blomgren et al., U.S. Patent Number 5,685,009 (herein referred to as '009), and U.S. Patent Number 5,781,750 (herein referred to as '750) incorporated by reference into '009 at column 3, lines 44-47. The shared registers disclosed in '009 are for use in the device disclosed in '750, as shown in '009 in column 1, line 24 to column 2, line 33; column 3, lines 444-67; and column 4, lines 6-16, hence '750 is incorporated by reference in '009 in the same embodiment.

18. Referring to claim 2, Guenthner has not explicitly taught the multi-mode processor of Claim 1 wherein the mode identifier is one of a plurality of bits in a processor status register. However, Guenthner has taught that the mode is determined in the decoder (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..."), but does not teach the details of the decoder or how it determines the mode. Blomgren has taught a decoder in a multi-mode processor whose mode identifier is one of a plurality of bits in a processor status register ('750 column 3, line 65 to column 4, line 2 "...A select means, coupled to the first instruction decode means and the second instruction decode means..."; column 4, lines 7-11 "...a mode register indicates whether the first or the second instruction set is currently being processed..."; column 6, lines 53-57 "...Multiplexer of MUX

46 selects the decoded instruction..."; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that '750's decoder provides correct decoding for proper execution of instructions fro different instruction sets, thereby ensuring correct execution of instructions. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the decoder of '750 in the device of Guenthner to ensure the correct execution of instructions.

19. Referring to claim 5, Guenthner in view of '009 and '750 have taught the multi-mode processor of Claim 1 wherein the input may contain a token (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, the decoder distinguishes which instruction set is being executed and routes it accordingly to a processing unit.), wherein the floating-point registers are 82 bits wide ('009 column 2, lines 13-22 "Wider formats for floating point data are typically used...Often 64 or 80-bit formats are used for floating point numbers..."), and wherein the token being an 82 bit processor known value ('009 column 1, lines 43-47 "...Two instruction decoders are required when the instruction sets are separate..." and column 2, lines 13-22 "Wider formats for floating point data are typically used...Often 64 or 80-bit formats are used for floating point numbers..." and 51-58 "A first means is for accessing the shared register..."; and '750 column 3, line 65 to column 4, line 21 "...A select means, coupled to the first instruction decode means and the second instruction decode means..."; column 6, lines 53-59 "...Multiplexer of MUX **46** selects the decoded instruction..."; column 7, lines 30-54 "Mode control logic **42** causes emulation mode to be entered whenever a miss is signaled..."; and Figure 2).

20. Referring to claim 7, Guenthner in view of '009 and '750 have taught the multi-mode processor of Claim 1 wherein the floating point registers each comprise:

a. A sign bit ('009 column 2, lines 12-22 "...Floating-point numbers include a fraction or mantissa portion and an exponent portion..." – In regard to '009, it is inherent that the significand, also known as the mantissa, includes the sign bit. Please see FOLDOC definition mantissa © 1996 provided with the Office Action dated 30 June 2003.),

b. An exponent ('009 column 2, lines 12-22 "...Floating-point numbers include a fraction or mantissa portion and an exponent portion..."); and

c. A significand ('009 column 2, lines 12-22 "...Floating-point numbers include a fraction or mantissa portion and an exponent portion...".

21. Referring to claim 11, Guenthner in view of '009 and '750 have taught the method of Claim 10 wherein the input is comprised of at least one operand and at least one operator (Guenthner column 3, lines 22-63 "The instruction cache **56** is coupled to and provides instructions to an instruction execution unit **52**..." – In regards to Guenthner, instructions inherently have at least one operand and at least one operator. Please see the accompanying information about instructions.); wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token ('009 column 1, lines 43-47 "...Two instruction decoders are required when the instruction sets are separate..." and column 2, lines 51-58 "A first means is for accessing the shared register..."; and '750 column 3, line 65 to column 4, line 21 "...A select means, coupled to the first instruction decode means and the second instruction decode means..."; column 6, lines 53-59 "...Multiplexer of MUX **46** selects

the decoded instruction..."; column 7, lines 30-54 "Mode control logic **42** causes emulation mode to be entered whenever a miss is signaled..."; and Figure 2); and wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode ('009 column 1, lines 43-47 "...Two instruction decoders are required when the instruction sets are separate..." and column 2, lines 51-58 "A first means is for accessing the shared register..."; and '750 column 3, line 65 to column 4, line 21 "...A select means, coupled to the first instruction decode means and the second instruction decode means..."; column 6, lines 53-59 "...Multiplexer of MUX **46** selects the decoded instruction..."; column 7, lines 30-54 "Mode control logic **42** causes emulation mode to be entered whenever a miss is signaled..."; and Figure 2).

22. Referring to claim 13, Guenthner in view of '009 and '750 have taught the method of Claim 10 wherein performing comprises propagating the token ('009 column 3, lines 57-67 "The third mode of operation..."; and '750 column 5, line 49 to column 6, line 13 "Emulation mode..."); and wherein producing output comprises setting the output to be the token ('009 column 3, lines 57-67 "The third mode of operation..."; and '750 column 5, line 49 to column 6, line 13 "Emulation mode..." – In regards to '009 and '750, the indication that the CPU is in emulation mode must be propagated through the entire process of switching from CISC to RISC and back to CISC.).

23. Referring to claim 16, Guenthner in view of '009 and '750 have taught the method of Claim 10 wherein checking comprises checking a mode identifier (Guenthner column 5, lines 46-55 "...efficiently distinguish the two (or more) types of instructions that can execute..." – In regards to Guenthner, a mode identifier is whatever the decoder uses to identify which

instruction set the current instruction is from.) bit in a processor status register ('750 column 3, line 65 to column 4, line 2 "...A select means, coupled to the first instruction decode means and the second instruction decode means..."; column 4, lines 7-11 "...a mode register indicates whether the first or the second instruction set is currently being processed..."; column 6, lines 53-57 "...Multiplexer of MUX **46** selects the decoded instruction..."; and Figure 2).

24. Referring to claims 6 and 14, Guenthner, U.S. Patent Number 6,448,676 (herein referred to as Guenthner), as applied to claims 1 and 10 above, further in view of Blomgren et al., U.S. Patent Number 5,685,009 (herein referred to as '009), and U.S. Patent Number 5,781,750 (herein referred to as '750) incorporated by reference into '009 at column 3, lines 44-47, and in further view of InstantWeb's Online Computing Dictionary terms "speculative evaluation" and "speculative execution" (herein referred to as FOLDOC).

25. Guenthner in view of '009 and '750 have taught wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful load request ('750 column 4, lines 13-33 and column 7, lines 25-32). In regards to '750, the TLB is used to load the physical address of the instruction when virtual addresses are present and emulation mode is entered when a miss occurs in the TLB, i.e. cannot find the physical address to load, thereby creating an unsuccessful load request. FOLDOC has taught speculative evaluation and execution of instructions (FOLDOC terms "speculative evaluation" and "speculative execution"). A person of ordinary skill in the art at the time the invention was made would have recognized that speculative evaluation and execution reduces the overall run-time of a process and keeps all functional units working, i.e. not wasted cycles, (FOLDOC terms "speculative evaluation" and "speculative execution"), thereby increasing processor speed and efficiency. Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to incorporate the speculative evaluation and execution of FOLDOC in the device of '009 and '750 to improve processor speed and efficiency.

Response to Arguments

26. Examiner withdraws the claim objection in favor of the amended claims.

27. Examiner withdraws the claim rejections under 35 U.S.C. §112 in favor of the amended claims.

28. Examiner withdraws the claim rejection under 35 U.S.C. §101 in favor of the amended claims.

29. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Kanamori et al., U.S. Patent Numbers 5,734,904 and 6,438,621, have taught a system with multiple word size modes, such as 16-bit mode and 32-bit mode.

b. Fredrickson, U.S. Patent Number 5,757,826, has taught switching between 8 and 16 bit wide datapaths.

c. Guenthner, U.S. Patent Number 6,230,256, is from the same patent family as the Guenthner patent used in the rejection above and teaches similar elements.

d. Huck et al., U.S. Patent Number 6,408,380, has taught floating point instructions having values with different word sizes.

e. Adusumilli, U.S. Patent Number 6,438,700, and Jaggar et al., U.S. Patent Number 6,446,221, have taught switching between ARM, a larger word size instruction set, and THUMB, a smaller word size instruction set and floating point operations.

31. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

32. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Examiner
Art Unit 2183

31 May 2007

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